

Patent claims

1. A metallization arrangement for a semiconductor structure (1) having:
- 5 a first substructure plane (M1);
a second metallization plane (M2) having a first and a second adjacent interconnect (LBA; LBB);
a first intermediate dielectric (ILD1) for mutual electrical insulation of the first substructure plane (M1) and second metallization plane (M2);
10 and
via holes (V) filled with a conductive material (FM) in the intermediate dielectric (ILD1) for connecting the first substructure plane (M1) and
15 second metallization plane (M2);
a liner layer (L) made of a dielectric material being provided under the second metallization plane (M2), which liner layer is interrupted in the interspace (O) between the first and second
20 adjacent interconnects (LBA; LBB) of the second metallization plane (M2).
2. The metallization arrangement as claimed in claim 1,
25 wherein
the first substructure plane (M1) is a first metallization plane.
3. The metallization arrangement as claimed in claim 1 or 2,
30 wherein
the interspace (O) between the first and second adjacent interconnects (LBA; LBB) of the second metallization plane (M2) is filled with a second
35 intermediate dielectric (ILD2) above the first intermediate dielectric (ILD1).

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4. The metallization arrangement as claimed in claim
1, 2 or 3,
wherein
the semiconductor structure has an electrical
circuit integrated in a silicon substrate.

5. The metallization arrangement as claimed in one of
claims 1 to 4,
wherein
10 the liner layer (L) is fabricated from silicon
dioxide or silicon nitride.

6. The metallization arrangement as claimed in one of
claims 2 to 4,
15 wherein
the first and/or second metallization plane (M1;
M2) are/is fabricated from AlCu.

7. A method for fabricating a metallization arrangement for a semiconductor structure (1) having the steps of:
providing a first substructure plane (M1), preferably a first metallization plane, on the semiconductor structure (1);
providing a first intermediate dielectric (ILD1) on the first substructure plane (M1);
providing a liner layer (L) made of a dielectric material on the first substructure plane (M1);
providing via holes (V) filled with a conductive material (FM) in the first intermediate dielectric (ILD1) and the liner layer (L);
providing a second metallization plane (M2) on the resulting structure;
patterning a first and a second adjacent interconnect (LBA; LBB) in the second metallization plane (M2); and interrupting the liner layer in the interspace (O) between the

first and second adjacent interconnects (LBA; LBB) of the second metallization plane (M2).

- 5 8. The method as claimed in claim 7,
wherein
the patterning and interrupting are carried out in
a common etching step.
- 10 9. The method as claimed in claim 7 or 8,
wherein
the semiconductor structure has an electrical
circuit integrated in a silicon substrate.
- 15 10. The method as claimed in claim 9,
wherein
the liner layer (L) is fabricated from silicon
dioxide or silicon nitride.
- 20 11. The method as claimed in claim 10,
wherein
the patterning is carried out in a first metal
etching step and the interrupting is carried out
in a second silicon dioxide etching step.
- 25 12. The method as claimed in one of claims 7 to 11,
wherein
the interspace (O) between the first and second
adjacent interconnects (LBA; LBB) of the second
metallization plane (M2) is filled with a second
30 intermediate dielectric (ILD2) above the first
intermediate dielectric (ILD1).
- 35 13. The method as claimed in one of claims 7 to 12,
wherein
a hard mask or a resist mask, which is provided on
the second metallization plane (M2), is used for
the patterning and interrupting processes.

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